Reg.No.:												

VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN
[AUTONOMOUS INSTITUTION AFFILIATED TO ANNA UNIVERSITY, CHENNAI]
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Question Paper Code: 50023

B.E. / B.Tech. DEGREE END-SEMESTER EXAMINATIONS – NOV. / DEC. 2025
Third Semester
Computer Science and Engineering
U23CS305 – COMPUTER ORGANIZATION AND ARCHITECTURE
(Common to IT, CST and AI&DS)
(Regulation 2023)

Time: Three Hours | Maximum: 100 Marks

Answer ALL the questions

Knowledge Levels (KL)	K1 – Remembering	K3 – Applying	K5 - Evaluating
	K2 – Understanding	K4 – Analyzing	K6 - Creating

PART – A

(10 x 2 = 20 Marks)

Q.No.	Questions	Marks	KL	CO
1.	Name any four common types of registers used in a CPU.	2	K1	CO1
2.	Given the simple instruction ADD A, B, write how the control unit would coordinate with the ALU and memory to execute it.	2	K2	CO1
3.	Analyze the usefulness of immediate addressing in program execution.	2	K2	CO2
4.	Compare register-to-register data transfer with memory-to-register data transfer in terms of speed and instruction execution.	2	K2	CO2
5.	Compare the relative advantages of floating-point representation over fixed-point number representation in computers.	2	K2	CO3
6.	Write two important advantages of using 2's complement representation in computers instead of the sign-magnitude representation.	2	K2	CO3
7.	In DMA, data transfer occurs between which two units of a computer?	2	K1	CO4
8.	Analyze the impact of cache line size on memory access efficiency.	2	K2	CO4
9.	Write any two important differences between an instruction pipeline and an arithmetic pipeline.	2	K2	CO5
10.	Almost no commercially available multicore processor supports shared L1 cache. Identify two important shortcomings of shared L1 caches as compared to private L1 caches.	2	K2	CO5

PART – B

(5 x 13 = 65 Marks)

Q.No.		Questions	Marks	KL	CO
11.	a)	Explain the role of instruction codes and computer registers in the execution of a program. Describe the steps of the instruction cycle, and discuss how timing and control signals coordinate these operations.	13 (5+8)	K2	CO1
		(OR)			
	b)	With the help of a block diagram, explain how the important units of a computer system are interconnected in a bus-based architecture.	13	K2	CO1
12.	a)	Differentiate between immediate, direct, and indirect addressing modes of instruction operands with examples.	13	K2	CO2
		(OR)			
	b)	Draw a comparison table, showing at least five differences between RISC and CISC architectures.	13	K2	CO2
13.	a)	Analyze the effectiveness of Booth's algorithm for signed multiplication compared to the simple shift-and-add method. In your answer, identify the situations where Booth's algorithm provides performance benefits and where it may introduce inefficiencies."	13 (8+5)	K3	CO3
		(OR)			
	b)	Differentiate between arithmetic, logic, and shift micro-operations with examples.	13	K3	CO3
14.	a)	Analyze how Direct Memory Access (DMA) improves system performance compared to programmed I/O and interrupt-driven I/O. In your answer, discuss the trade-offs in terms of CPU utilization, data transfer speed, and system complexity, using the block diagram of DMA as reference.	13 (5+8)	K3	CO4
		(OR)			
	b)	Explain the principle of locality and how cache memory uses this to improve CPU performance. Compute average memory access time if cache hit time=1 clock cycle, cache miss penalty is 100 clock cycles, and hit ratio=90%.	13 (5+8)	K3	CO4
15.	a)	Draw a schematic of a vector processor and analyze how vector processors achieve higher performance in scientific and engineering applications compared to scalar processors. In your answer, discuss the role of data-level parallelism, memory bandwidth requirements, and limitations such as vector length dependency.	13 (8+5)	K2	CO5
		(OR)			

	b)	Draw a schematic showing how caches are connected to the processors in a multicore processor architecture. With its help, analyze the issues of cache coherence and inter-core communication in a multicore processor.	13 (5+8)	K2	CO5

PART – C

(1 x 15 = 15 Marks)

Q.No.		Questions	Marks	KL	CO
16.	a)	Analyze why increasing the complexity of an instruction set (CISC approach) does not necessarily translate into higher processor performance. Based on your analysis, justify why high-performance computing tasks like weather forecasting are better suited to parallel processors rather than general-purpose CISC machines.	15 (5+10)	K3	CO5
		(OR)			
	b)	Analyze how different types of data dependencies (RAW, WAR, WAW) affect instruction throughput in a pipelined processor. Evaluate the effectiveness of hardware-based solutions (such as forwarding and hazard detection) versus compiler-based approaches (such as instruction scheduling) in minimizing pipeline stalls.	15 (7+8)	K3	CO5